

1:10 Clock Fanout Buffer

Features

- Low voltage operation
- Full range support:
 - 3.3 V
 - 2.5 V
 - 1.8 V
- Over voltage tolerant input hot swappable
- 1:10 Fanout
- Drives either a 50-Ohm or 75-Ohm load
- Low input capacitance
- Low output skew
- Low propagation delay
- Typical (t_{pd} less than 4 ns)
- High speed operation:
 - 200 MHz at 1.8 V
 - 650 MHz at 2.5 V and 3.3 V

- Industrial temperature range
- Available in SSOP package

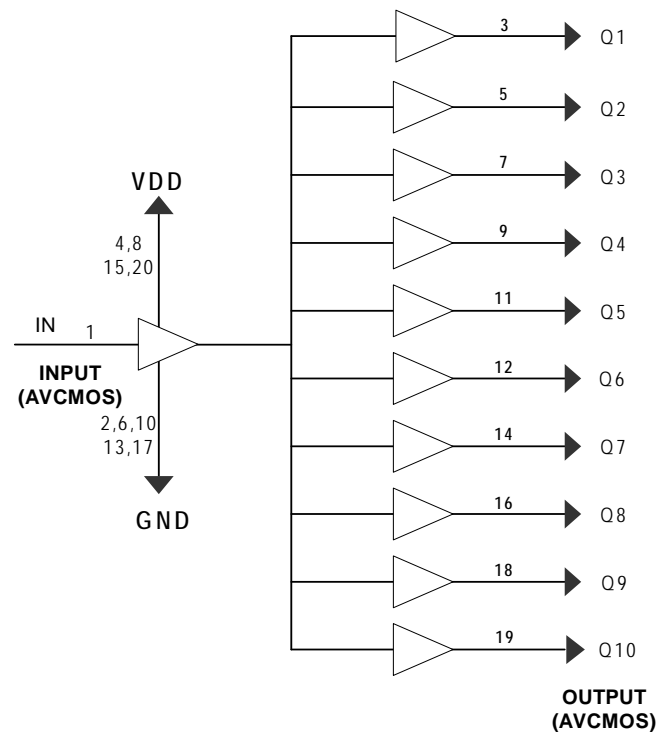
Description

The Cypress series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC910 fanout buffer features one input and 10 outputs. It is ideal for conversion from and to 3.3 V, 2.5 V, and 1.8 V

Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.

Logic Block Diagram

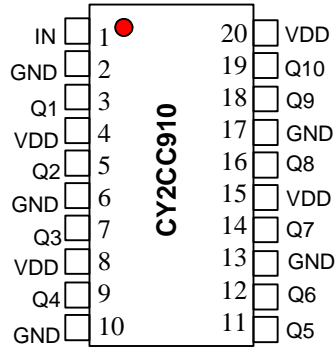


Contents

| | | | |
|--|----------|--|-----------|
| Features | 1 | AC Switching Characteristics | 5 |
| Description | 1 | AC Switching Characteristics | 6 |
| Logic Block Diagram | 1 | Parameter Measurement Information: | |
| Contents | 2 | VDD at 3.3 V to 2.5 V | 6 |
| Pin Configuration | 2 | Parameter Measurement Information: VDD at 8 V | 7 |
| Pin Description | 2 | Ordering Code Definitions | 8 |
| Maximum Ratings ^[1] | 2 | Package Drawing | 9 |
| Variable Output Impedance Control (VOI) | 3 | Acronyms | 10 |
| DC Electrical Characteristics | 3 | Document Conventions | 10 |
| At 3.3 V | 3 | Document History Page | 11 |
| At 2.5 V | 4 | Sales, Solutions, and Legal Information | 12 |
| At 1.8 V | 4 | Worldwide Sales and Design Support | 12 |
| Capacitance | 4 | Products | 12 |
| Power Supply Characteristics | 4 | PSoC Solutions | 12 |
| High Frequency Parametrics | 5 | | |

Pin Configuration

Figure 1. 20-Pin SOIP-SSOP



20 pin SOIC/SSOP

Pin Description

| Pin Number | Pin Name | Description |
|---------------------------|--------------------------------|--------------|
| 1 | IN | Input |
| 2,6,10,13,17 | GND | Ground |
| 4,8,15,20 | V _{DD} | Power Supply |
| 3,5,7,9,11,12,14,16,18,19 | Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,Q9,Q10 | Output |

Maximum Ratings^[1]

Storage temperature:..... -65° C to +150° C
 Ambient temperature:..... -40° C to +85° C
 Supply voltage to ground potential
 V_{CC}.....-0.5 V to 4.6 V
 Input.....-0.5 V to 5.8 V

Supply voltage to ground potential
 (Outputs only)..... -0.5 V to V_{DD} + 1 V
 DC output voltage..... -0.5 V to V_{DD} + 1 V
 Power dissipation 0.75 W

Note

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Variable Output Impedance Control (VOI)

DC Electrical Characteristics

At 3.3 V (See Figure 2)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|--------------------------|--|-----|------|------|---------------|
| V_{OH} | Output high voltage | $V_{DD} = \text{Min}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -12 \text{ mA}$ | 2.3 | 3.3 | | V |
| V_{OL} | Output low voltage | $V_{DD} = \text{Min}, V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 12 \text{ mA}$ | | 0.2 | 0.5 | V |
| V_{IH} | Input high voltage | Guaranteed Logic High Level | 2 | | 5.8 | V |
| V_{IL} | Input low voltage | Guaranteed Logic Low Level | | | 0.8 | V |
| I_{IH} | Input high current | $V_{DD} = \text{Max}$ $V_{IN} = 2.7 \text{ V}$ | | | 1 | μA |
| I_{IL} | Input low current | $V_{DD} = \text{Max}$ $V_{IN} = 0.5 \text{ V}$ | | | -1 | μA |
| I_I | Input high current | $V_{DD} = \text{Max}, V_{IN} = V_{DD}(\text{Max})$ | | | 20 | μA |
| V_{IK} | Clamp diode voltage | $V_{DD} = \text{Min}, I_{IN} = -18 \text{ mA}$ | | -0.7 | -1.2 | V |
| I_{OK} | Continuous clamp current | $V_{DD} = \text{Max}, V_{OUT} = \text{GND}$ | | | -50 | mA |
| O_{OFF} | Power-down disable | $V_{DD} = \text{GND}, V_{OUT} = < 4.5 \text{ V}$ | | | 100 | μA |
| V_H | Input hysteresis | | | 80 | | mV |

Note

2. Test load conditions: 500-Ohm to ground with approximately 6-pF total loading and 200-MHz maximum frequency.

At 2.5 V (See Figure 2)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------|---|-------------------------|------|------|------|
| V _{OH} | Output high voltage | V _{DD} = Min, V _{IN} = V _{IH} or V _{IL} | I _{OH} = -7 mA | 1.8 | | V |
| | | | I _{OH} = 12 mA | 1.6 | | V |
| V _{OL} | Output low voltage | V _{DD} = Min, V _{IN} = V _{IH} or V _{IL} | | | 0.65 | V |
| V _{IH} | Input high voltage | Guaranteed Logic High Level | 1.6 | | 5.0 | V |
| V _{IL} | Input low voltage | Guaranteed Logic Low Level | | | 0.8 | V |
| I _{IH} | Input high current | V _{DD} = Max | | | 1 | μA |
| I _{IL} | Input low current | V _{DD} = Max | | | -1 | μA |
| I _I | Input high current | V _{DD} = Max, V _{IN} = V _{DD} (Max) | | | 20 | μA |
| V _{IK} | Clamp diode voltage | V _{DD} = Min, I _{IN} = -18 mA | | -0.7 | -1.2 | V |
| I _{OK} | Continuous clamp current | V _{DD} = Max, V _{OUT} = GND | | | -50 | mA |
| O _{OFF} | Power down disable | V _{DD} = GND, V _{OUT} = < 4.5 V | | | 100 | μA |
| V _H | Input hysteresis | | | 80 | | mV |

At 1.8 V (See Figure 6)

| Parameter | Description | Test Condition ^[2] | Min | Max | Unit |
|-----------------|---------------------|-------------------------------|-----------------------------|----------------------------|------|
| V _{DD} | Supply voltage | | 1.71 | 1.89 | V |
| V _{IH} | Input high voltage | | 0.65 V _{DD} [1.1] | 4.3 | V |
| V _{IL} | Input low voltage | | -0.3 | 0.35 V _{DD} [0.6] | V |
| V _{OH} | Output high voltage | I _{OH} = -2 mA | V _{DD} - 0.45[1.2] | | V |
| V _{OL} | Output low voltage | I _{OH} = 2 mA | | 0.45 | V |

Capacitance

| Parameter | Description | Test Conditions | Typ | Max | Unit |
|------------------|--------------------|------------------------|-----|-----|------|
| C _{IN} | Input capacitance | V _{IN} = 0 V | 2.5 | | pF |
| C _{OUT} | Output capacitance | V _{OUT} = 0 V | 6.5 | | pF |

Power Supply Characteristics (See Figure 2)

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|------------------|--|---|-----|-----|------|------------|
| ΔI _{CC} | Delta I _{CC} Quiescent Power Supply Current | (I _{DD} @ V _{DD} = Max and V _{IN} = V _{DD}) - (I _{DD} @ V _{DD} = Max and V _{IN} = V _{DD} - 0.6 V(6 V)) | | | 50 | μA |
| I _{CCD} | Dynamic power supply current | V _{DD} = Max Input toggling 50% Duty Cycle, Outputs Open | | | 0.63 | mA/ MHZ |
| I _C | Total power supply current | V _{DD} = Max Input toggling 50% Duty Cycle, Outputs Open f _L = 40 MHZ | | | 25 | mA |

High Frequency Parametrics

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---------------------------|--|--|-----|-----|-----|------|
| D _J | Jitter, Deterministic | 50% duty cycle t _W (50–50) The “point to point load circuit” Output Jitter – Input Jitter | | | 20 | ps |
| F _{max} 3.3 V | Maximum frequency V _{DD} = 3.3 V | 50% duty cycle t _W (50–50) Standard Load Circuit. | | | 160 | MHz |
| | | 50% duty cycle t _W (50–50) The “point to point load circuit” | | | 650 | |
| F _{max} 2.5 V | Maximum frequency V _{DD} = 2.5 V | The “point-to-point load circuit” V _{IN} = 2.4 V/0.0 V V _{OUT} = 1.7 V/0.7 V | | | 200 | MHz |
| F _{max} 1.8 V | Maximum frequency V _{DD} = 1.8 V | The “6-pF load circuit” V _{IN} = 1.7/0.0 V V _{OUT} = 1.2 V/0.4 V | | | 200 | MHz |
| F _{max(20)} | Maximum frequency V _{DD} = 3.3 V | 20% duty cycle t _W (20–80) The “point to point load circuit” V _{IN} = 3.0 V/0.0 V V _{OUT} = 2.3 V/0.4 V | | | 250 | MHz |
| t _W 3.3 V | Minimum pulse V _{DD} = 3.3 V | The “point-to-point load circuit” V _{IN} = 3.0 V/0.0 V F = 100 MHz V _{OUT} = 2.0 V/0.8 V | 1 | | | ns |
| t _W 2.5 V | Minimum pulse V _{DD} = 2.5 V | The “point-to-point load circuit” V _{IN} = 2.4 V/0.0 V F = 100 MHz V _{OUT} = 1.7 V/0.7 V | 1 | | | ns |
| t _W 1.8 V | Minimum pulse V _{DD} = 1.8 V | The “6-pF load circuit” V _{IN} = 1.7 V/0.0 V V _{OUT} = 1.2 V/0.4 V | 1 | | | ns |

AC Switching Characteristics

At 3.3 V (V_{DD} = 3.3 V ± 5%, Temperature = –40° C to +85° C)

| Parameter | Description | Min | Typ | Max | Unit | |
|--------------------|--|---------------|-----|-----|------|------|
| t _{PLH} | Propagation delay – Low to High | See Figure 3 | 1.5 | 2.7 | 3.5 | ns |
| t _{PHL} | Propagation delay – High to Low | | 1.5 | 2.7 | 3.5 | ns |
| t _R | Output rise time | | | 0.8 | | V/ns |
| t _F | Output fall time | | | 0.8 | | V/ns |
| t _{SK(0)} | Output Skew: Skew between outputs of the same package (in phase). | See Figure 10 | | | 0.2 | ns |
| t _{SK(p)} | Pulse Skew: Skew between opposite transitions of the same output (t _{PHL} – t _{PLH}). | See Figure 9 | | | 0.2 | ns |
| t _{SK(t)} | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | See Figure 11 | | | 0.4 | ns |

At 2.5 V (V_{DD} = 2.5 V ± 5%, Temperature = –40 ° C to +85 ° C)

| Parameter | Description | Min | Typ | Max | Unit | |
|--------------------|--|---------------|-----|-----|------|------|
| t _{PLH} | Propagation delay – Low to High | See Figure 3 | 1.5 | 2.7 | 3.5 | ns |
| t _{PHL} | Propagation delay – High to Low | | 1.5 | 2.7 | 3.5 | ns |
| t _R | Output rise time | | | 0.8 | | V/ns |
| t _F | Output fall time | | | 0.8 | | V/ns |
| t _{SK(0)} | Output Skew: Skew between outputs of the same package (in phase). | See Figure 10 | | | 0.2 | ns |
| t _{SK(p)} | Pulse Skew: Skew between opposite transitions of the same output (t _{PHL} – t _{PLH}). | See Figure 9 | | | 0.2 | ns |
| t _{SK(t)} | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | See Figure 11 | | | 0.4 | ns |

AC Switching Characteristics

At 1.8 V ($V_{DD} = 1.8 \text{ V} \pm 5\%$, Temperature = -40°C to $+85^\circ \text{C}$)

| Parameter | Description | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| t_{PLH} | Propagation delay – Low to High | 1.5 | 2.7 | 3.5 | ns |
| t_{PHL} | Propagation delay – High to Low | 1.5 | 2.7 | 3.5 | ns |
| t_R | Output rise time 20 – 80% | 0.2 | | 1.5 | ns |
| t_F | Output fall time 20 – 80% | 0.2 | | 1.5 | ns |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase). | | | 0.2 | ns |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$). | | | 0.2 | ns |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | | | 0.4 | ns |

Parameter Measurement Information: V_{DD} at 3.3 V to 2.5 V

Figure 2. Load Circuit [3,4,5]

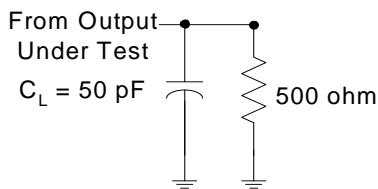


Figure 4. Point to Point Load Circuit [3,4,5]

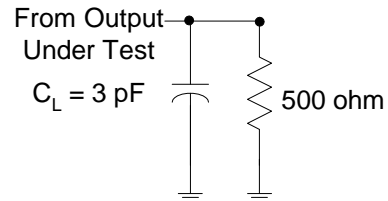


Figure 3. Voltage Waveforms Propagation Delay Times [6]

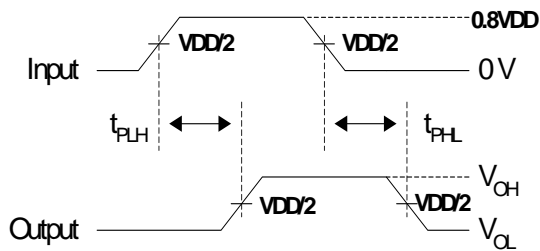
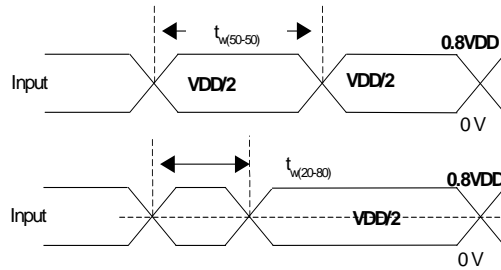


Figure 5. Voltage Waveforms – Pulse Duration [4]



Parameter Measurement Information: V_{DD} at 8 V

Figure 6. Load Circuit [3,4,5]

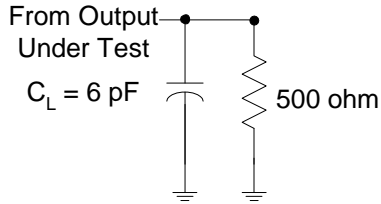


Figure 8. Voltage Waveforms – Pulse Duration^[4]

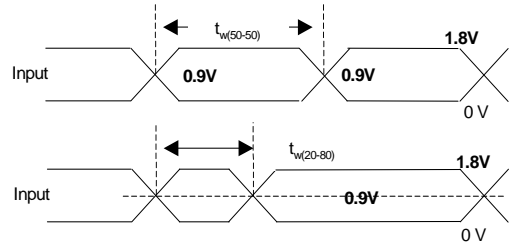


Figure 7. Voltage Waveforms Propagation

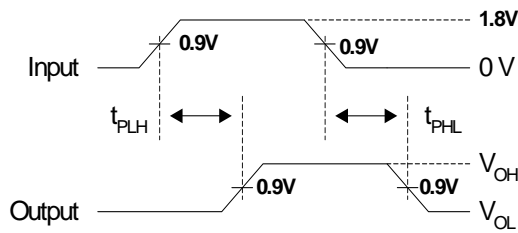


Figure 9. Pulse Skew - $tsk_{(p)}$

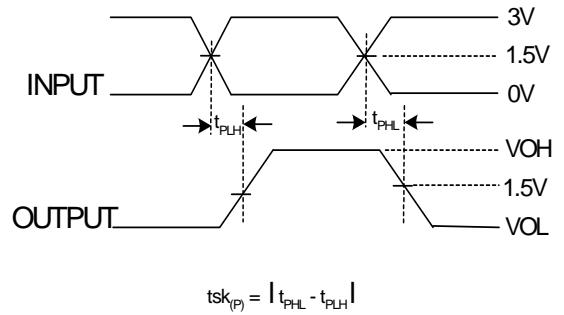
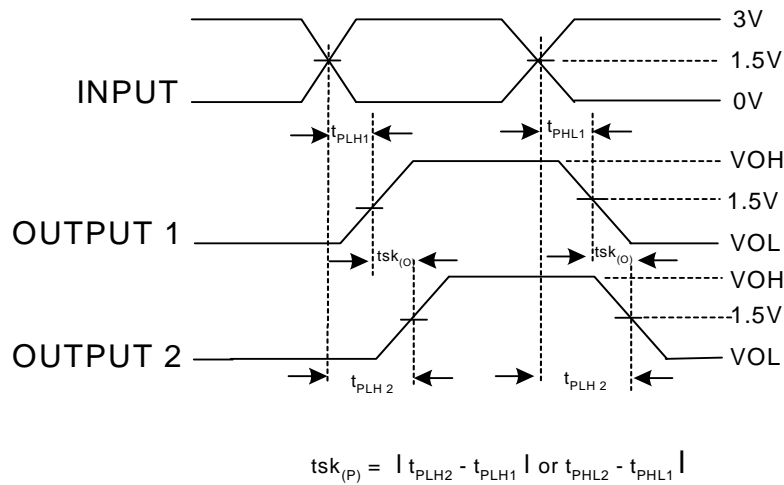


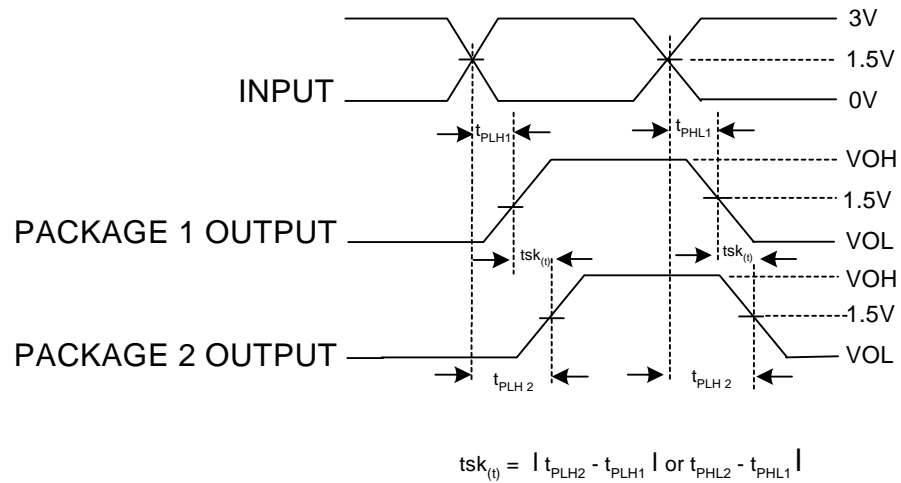
Figure 10. Output Skew - $tsk_{(o)}$



Notes

3. C_L includes probe and jig capacitance.
4. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, $Z_0 = 50\Omega$, $t_R < 2.5 \text{ ns}$, $t_F < 2.5 \text{ ns}$.
5. The outputs are measured one at a time with one transition per measurement.
6. T_{PLH} and T_{PHL} are the same as t_{pd} .

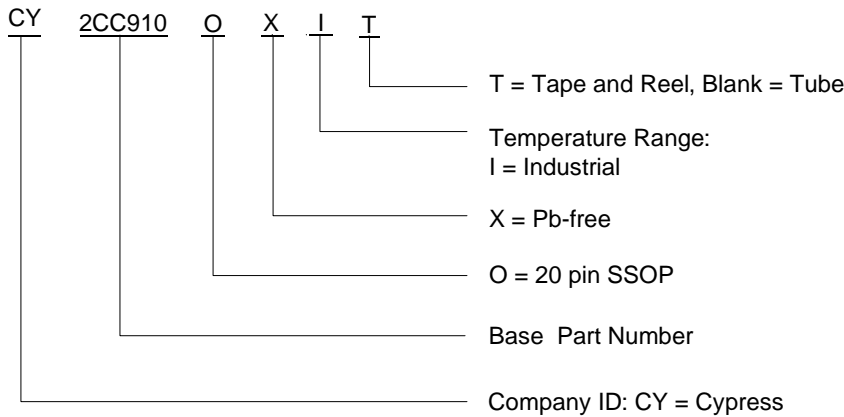
Figure 11. Package Skew - $tsk_{(t)}$



Ordering Information

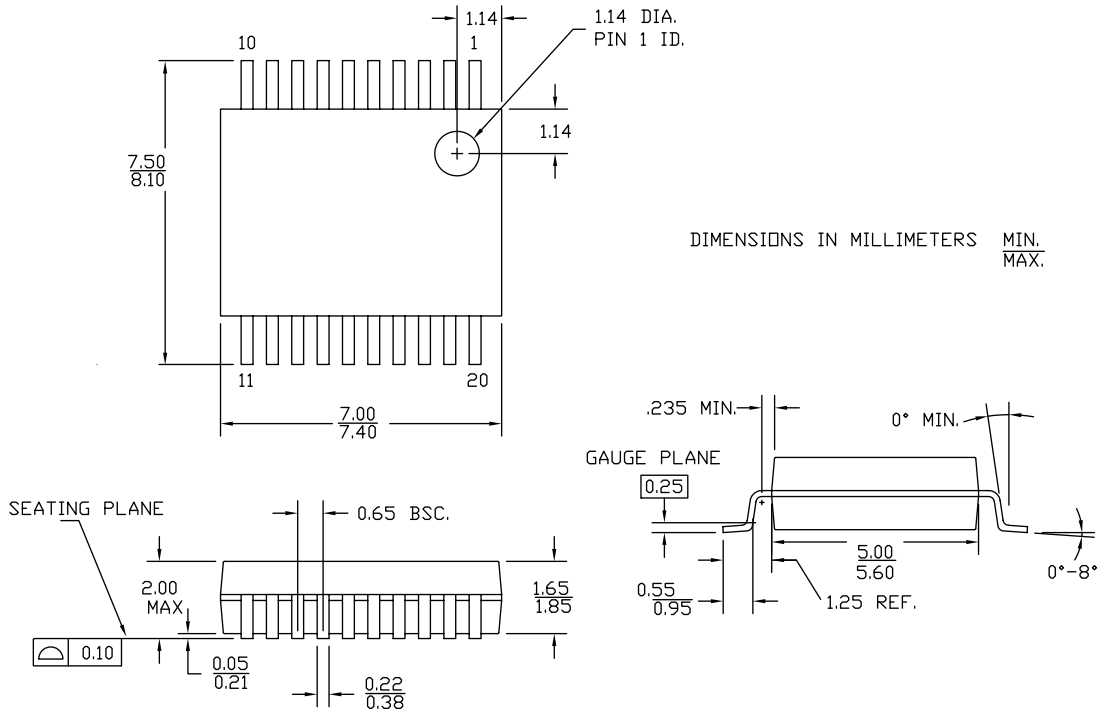
| Part Number | Package Type | Product Flow |
|----------------|---------------------------|-----------------------------|
| Pb-free | | |
| CY2CC910OXI | 20-pin SSOP | Industrial, -40° C to 85° C |
| CY2CC910OXIT | 20-pin SSOP-Tape and Reel | Industrial, -40° C to 85° C |

Ordering Code Definitions



Package Drawing

Figure 12. 20-Pin Shrunk Small Outline Package O20



51-85077 *E

Acronyms

| Acronym | Description |
|---------|---|
| CMOS | complementary metal oxide semiconductor |
| DJ | deterministic jitter |
| SSOP | shrunk small outline package |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| ° C | degree Celsius |
| MHZ | megahertz |
| uA | microamperes |
| mA | milliamperes |
| ms | milliseconds |
| ns | nanoseconds |
| % | percent |
| pF | picofarads |
| ps | picoseconds |
| V | volt |

Document History Page

| Document Title: CY2CC910 1:10 Clock Fanout Buffer Document No: 38-07348 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN NO. | Orig. of Change | Submission Date | Description of Change |
| ** | 114318 | TSM | 05/10/02 | New Data Sheet |
| *A | 119148 | RGL | 10/07/02 | Added 5.8 as the Max value for V_{IH} in the DC Electrical Characteristics @3.3 V table. Changed the Max value of V_{IH} from 5.8 to 5.0 in the DC Electrical Characteristics @2.5 V table. Changed the value of V_{IH} from $V_{DD}+0.3$ [2.25] to 4.3 in the DC Electrical Characteristics @1.8 V table. |
| *B | 404287 | RGL | See ECN | Added Lead-free devices for SSOP |
| *C | 2595534 | CXQ/PYRS | 10/23/08 | Added "Status" column to Ordering Information table Updated Package Diagram 51-85024 Updated template |
| *D | 2896073 | CXQ | 03/19/10 | Updated package diagram Removed obsolete parts from ordering information table and added CY2CC910OXI-1, CY2CC910OXI-1T Removed reference to SOIC packages |
| *E | 3056154 | CXQ | 10/08/2010 | Removed CY2CC910OXI-1, CY2CC910OXI-1T, CY2CC910OXC, and CY2CC910OXCT parts Ordering Information . Removed Note 7. |
| *F | 3411742 | PURU | 10/18/2011 | Added Contents , Acronyms , and Document Conventions Updated Package Drawing Removed Figure 2 Updated Ordering Information The statement related to Variable output impedance "Cypress employs the unique AVCMOS type outputs VOI (Variable Output Impedance) that dynamically adjust for variable impedance matching, eliminate the need for series damping resistors, and reduce overall noise." was removed. |

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