- **Distributes One Differential Clock Input to One LVPECL Differential Clock Output and One LVCMOS Single-Ended Output**
- **Programmable Output Divider for Both LVPECL and LVCMOS Outputs**
- **1.6-ns Output Skew Between LVCMOS and LVPECL Transitions Minimizing Noise**
- **3.3-V Power Supply (2.5-V Functional)**
- **Signaling Rate Up to 800-MHz LVPECL and 200-MHz LVCMOS**
- **Differential Input Stage for Wide Common-Mode Range Also Provides VBB Bias Voltage Output for Single-Ended Input Signals**
- **Receiver Input Threshold ±75 mV**
- **16-Pin QFN Package (3 mm x 3 mm)**

QFN PACKAGE
(TOP VIEW)

Pin	Name
16	EN
15	S1
14	Vss
13	S0
1	V_{DD}PECL
2	IN
3	$\overline{IN}$
4	VBB
5	Vss
6	Vss
7	Y1
8	Vdd1
9	$V_{DD}0$
10	Y0
11	$\overline{Y0}$
12	$V_{DD}0$
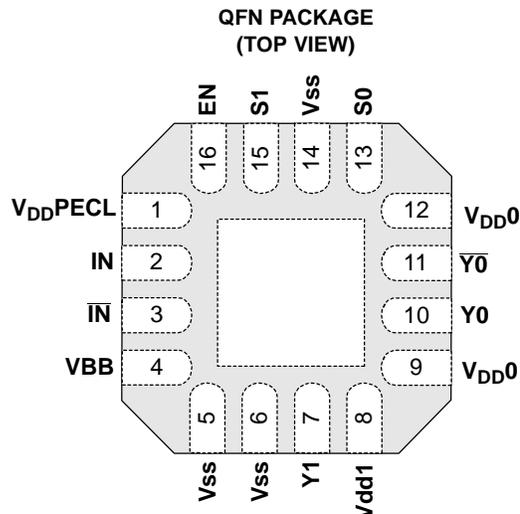
description

The CDCM1802 clock driver distributes one pair of differential clock input to one LVPECL differential clock output pair Y0 and $\overline{Y0}$ and one single-ended LVCMOS output Y1. It is specifically designed for driving 50-Ω transmission lines. The LVCMOS output is delayed by 1.6 ns over the PECL output stage to minimize noise impact during signal transitions.

The CDCM1802 has two control pins, S0 and S1, to select different output mode settings. The S[1:0] pins are 3-level inputs. Additionally, an enable pin EN is provided to disable or enable all outputs simultaneously. The CDCM1802 is characterized for operation from −40°C to 85°C.

For single-ended driver applications, the CDCM1802 provides a VBB output pin that can be directly connected to the unused input as a common-mode voltage reference.

TEXAS INSTRUMENTS

functional block diagram

Terminal Functions

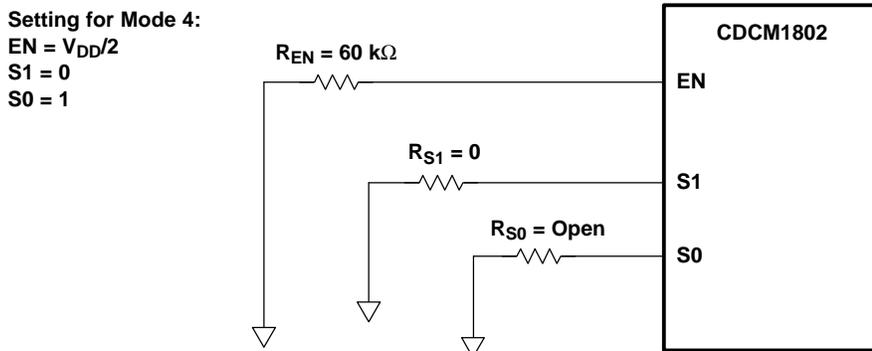| TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	16	I (with 60-kΩ pullup)	ENABLE. Enables or disables all outputs simultaneously; The EN pin offers three different configurations: tie to GND (logic 0), external 60-kΩ pulldown resistor (pull to $V_{DD}/2$) or left floating (logic 1); EN = 1: outputs on according to S0 and S1 setting EN = $V_{DD}/2$: outputs on according to S0 and S1 setting EN = 0; outputs Y[1:0] off (high-impedance) see Table 1 for details.
IN $\overline{\text{IN}}$	2 3	I Differential input	Differential input clock. Input stage is sensitive and has a wide common mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Since the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (e.g. with 100-Ω across input). The input can also be driven by a single-ended signal, if the complementary input is tied to a dc reference voltage (e.g. $V_{CC}/2$). The inputs deploy an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ~0.7 V. Reverse biasing of the IC through this inputs is possible and must be prevented by limiting the input voltage < VDD
S0 S1	13 15	I I (with 60-kΩ pullup)	Select mode of operation. Defines the output configuration of Y0 and Y1. Each pin offers three different configurations: tied to GND (logic 0), external 60-kΩ pulldown resistor (pull to $V_{DD}/2$) or left floating (logic 1); see Table 1 for details
Y1	7	O	LVCMOS clock output. This output provides a copy of IN or a divided down copy of clock IN based on the selected mode of operation: S0, S1, and EN. Also, this output can be disabled by tying $V_{DD}1$ to GND.
Y0 $\overline{\text{Y0}}$	10 11	O LVPECL	LVPECL clock output. This output provides a copy of IN or a divided down copy of clock IN based on the selected mode of operation: S1, S0, and EN. If Y0 output is unused, the output can simply be left open to save power and minimize noise impact to Y1.
VBB	4	O	Output bias voltage used to bias unused complementary input $\overline{\text{IN}}$ for single-ended input signals. The output voltage of VBB is V_{DD} –1.3 V. When driving a load, the output current drive is limited to about 1.5 mA.
V_{SS}	5, 6, 14	Supply	Device ground
V_{DD}PECL[1]	1	Supply	Supply voltage PECL input + internal logic
V_{DD}0[1]	9, 12	Supply	PECL output supply voltage for output Y0; Y0 can be disabled by pulling V_{DD}0 to GND. Caution: In this mode no voltage from outside may be forced because internal diodes could be forced in a forward direction. Thus, it is recommended to leave the output disconnect
V_{DD}1	8	Supply	Supply voltage CMOS output; The CMOS output can be disabled by pulling V_{DD}1 to GND. Caution: In this mode no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to leave Y1 unconnected, tied to GND or terminated into GND

NOTE 1: V_{DD}0, V_{DD}1, and V_{DD}PECL should have the same value.

control pin settings

The CDCM1802 has three control pins, S0, S1, and the enable pin (EN) to select different output mode settings. All three inputs (S0, S1, EN) are 3-level inputs. In addition, the EN input allows disabling all outputs and place them into a high-z (or tristate) output state when pulled to GND.

Setting for Mode 4:
$EN = V_{DD}/2$
$S1 = 0$
$S0 = 1$

$R_{EN} = 60$ kΩ

$R_{S1} = 0$

$R_{S0} = $ **Open**

CDCM1802

EN

S1

S0

Figure 1. Control Pin Setting for Example

Each control input incorporates a 60-kΩ pullup resistor. Thus, it is easy to choose the input setting by designing a resistor pad between the control input and GND. To choose a logic zero, the resistor value must be zero. Setting the input high requires leaving the resistor pad empty (no resistor installed). For setting the input to $V_{DD}/2$, the installed resistor needs a value of 60 kΩ with a tolerance better or equal to 10%.

Table 1. Selection Mode Table

				LVPECL	LVCMOS
MODE	EN	S1	S0	Y0	Y1
0	0	X	X	Off (high-z)	Off (high-z)
1	$V_{DD}/2$	0	$V_{DD}/2$	÷ 1	÷ 1
2	$V_{DD}/2$	$V_{DD}/2$	1	÷ 1	÷ 2
3	1	0	0	÷ 1	÷ 4
4	$V_{DD}/2$	0	1	÷ 2	÷ 2
5	1	0	1	÷ 2	÷ 4
6	$V_{DD}/2$	0	0	÷ 4	÷ 4
7	$V_{DD}/2$	1	0	÷ 4	÷ 8
8	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	÷ 8	÷ 1
9	1	1	0	÷ 8	÷ 4
10	1	1	1	Off (high-z)	÷ 4

NOTE: The LVPECL outputs are open emitter stages. Thus, if you leave the unused LVPECL output Y0 unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V_{DD} input to GND.

![Texas Instruments logo]
TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

V_{DD}	Supply voltage	–0.3 V to 3.8 V
V_I	Input voltage	–0.2 V to (V_{DD} +0.2 V)
V_O	Output voltage	–0.2 V to (V_{DD} +0.2 V)
Yn, $\overline{Yn}$, I_{OSD}	Differential short circuit current	Continuous
ESD	Electrostatic discharge (HBM 1.5 kΩ, 100 pF)	>2000 V
	Moisture level 16-pin QFN package (solder reflow temperature of 235°C) MSL	1
T_{stg}	Storage temperature	–65°C to 150°C
T_J	Maximum junction temperature	125°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Supply voltage, V_{DD} (only functionality)	2.375		3.6	V
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL INPUT IN, $\overline{IN}$						
f_{clk}	Input frequency		0		800	MHz
V_{CM}	High-level input common mode		1		V_{DD}–0.3	V
V_{IN}	Input voltage swing between IN and $\overline{IN}$, See Note 1		500		1300	mV
V_{IN}	Input voltage swing between IN and $\overline{IN}$, See Note 2		150		1300	mV
I_{IN}	Input current	$V_I = V_{DD}$ or 0 V			±10	µA
R_{IN}	Input impedance		300			kΩ
C_I	Input capacitance at IN, $\overline{IN}$			1		pF
LVPECL OUTPUT DRIVER Y0, $\overline{Y0}$						
f_{clk}	Output frequency, See Figure 4		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to V_{DD}–2 V	V_{DD}–1.18		V_{DD}–0.81	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to V_{DD}–2 V	V_{DD}–1.98		V_{DD}–1.55	V
V_O	Output voltage swing between Y and $\overline{Y}$, See Figure 4	Termination with 50 Ω to V_{DD}–2 V	500			mV
I_{OZL}	Output 3-state	V_{DD} = 3.6 V, V_O = 0 V			5	µA
I_{OZH}	Output 3-state	V_{DD} = 3.6 V, $V_O = V_{DD}$ – 0.8 V			10	µA
t_r/t_f	Rise and fall time	20% to 80% of V_{OUTPP}, see Figure 9	200		350	ps
t_{Duty}	Output duty cycle distortion, See Note 3	Crossing point-to-crossing point distortion	–50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y0, See Note A in Figure 8		50		ps
C_O	Output capacitance	$V_O = V_{DD}$ or GND		1		pF
LOAD	Expected output load			50		Ω

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL INPUT-TO-LVPECL OUTPUT PARAMETER						
$t_{pd(lh)}$	Propagation delay rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew, See Note B in Figure 8	VOX to VOX			100	ps

NOTES: 1. Is required to maintain ac specifications
2. Is required to maintain device functionality
3. For a 800-MHz signal, the 50-ps error would result into a duty cycle distortion of ±4% when driven by an ideal clock input signal.

LVCMOS OUTPUT PARAMETER, Y1

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clk}	Output frequency, see Note 4 and Figure 5			0		200	MHz
$t_{skLVCMOS(o)}$	Output skew between the LVCMOS output Y1 and LVPECL output Y0	VOX to V_{DD}/2, See Figure 8			1.6		ns
$t_{sk(pp)}$	Part-to-part skew	Y1, See Note A in Figure 8			300		ps
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 µA	V_{DD}–0.1			V
		V_{DD} = 3 V,	I_{OH} = –6 mA	2.4			
		V_{DD} = 3 V,	I_{OH} = –12 mA	2			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL}=100 µA			0.1	V
		V_{DD} = 3 V,	I_{OL} = 6 mA			0.5	
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.8	
I_{OH}	High-level output current	V_{DD} = 3.3 V,	V_O = 1.65 V		–29		mA
I_{OL}	Low-level output current	V_{DD} = 3.3 V,	V_O = 1.65 V		37		mA
I_{OZ}	High-impedance state output current	V_{DD} = 3.6 V,	V_O = V_{DD} or 0 V			±5	µA
C_O	Output capacitance	V_{DD} = 3.3 V			2		pF
Load	Expected output loading, see Figure 10				10		pF
t_{Duty}	Output duty cycle distortion, see Note 5	Measured at V_{DD}/2		–150		150	ps
$t_{pd(lh)}$	Propagation delay rising edge from IN to Y1	VOX to V_{DD}/2 load, see Figure 10		1.6		2.6	ns
$t_{pd(hl)}$	Propagation delay falling edge from IN to Y1	VOX to V_{DD}/2 load, see Figure 10		1.6		2.6	ns
t_r	Output rise slew rate	20% to 80% of swing, see Figure 10		1.4	2.3		V/ns
t_f	Output fall slew rate	80% to 20% of swing, see Figure 10		1.4	2.3		V/ns

NOTES: 4. Operating the CDCM1802 LVCMOS output above the maximum frequency will not cause a malfunction to the device, but the Y1 output signal swing will not achieve enough signal swing to meet the output specification. Therefore, the CDCM1802 can be operated at higher frequencies, while the LVCMOS output Y1 becomes unusable.
5. For a 200-MHz signal, the 150-ps error would result in a duty cycle distortion of ±3% when driven by an ideal clock input signal.

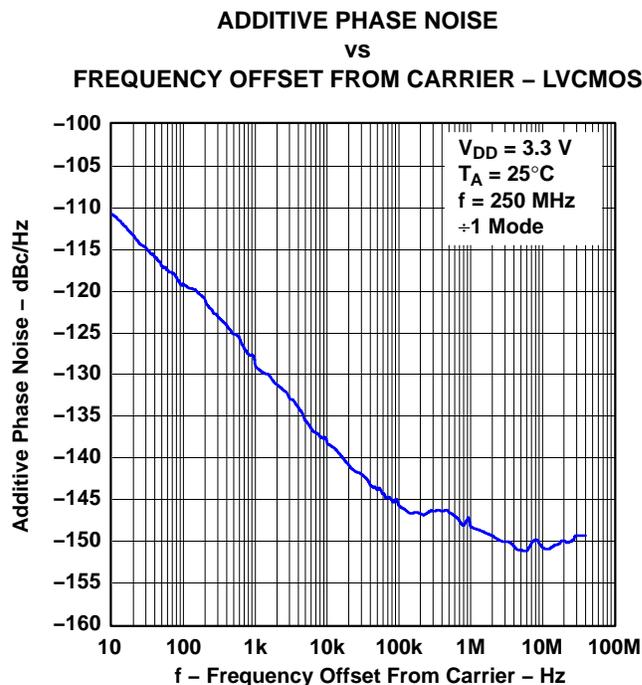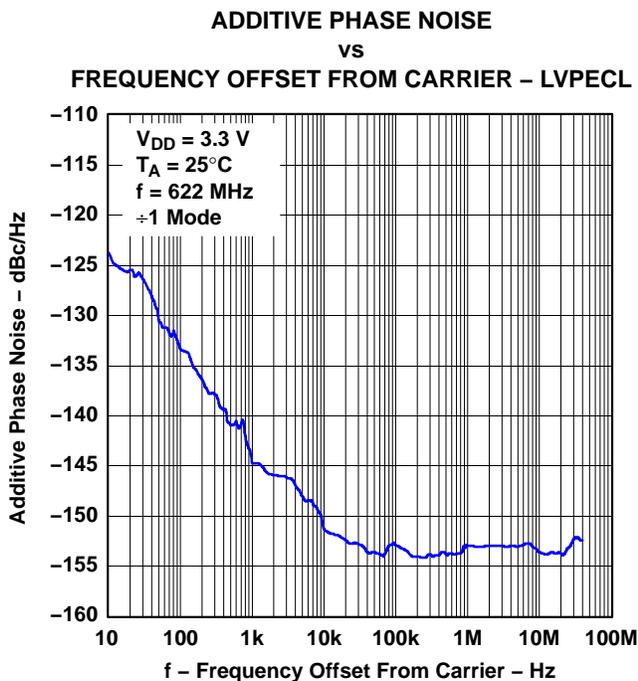## jitter characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output Y0, See Figure 2	12 kHz to 20 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.15	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz to 800 MHz, divide by 1 mode			0.25	
$t_{jitterLVCMOS}$	Additive phase jitter from input to LVCMOS output Y1, See Figure 3	12 kHz to 20 MHz, f_{out} = 250 MHz, divide by 1 mode			0.25	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz, divide by 1 mode			0.4	ps rms

ADDITIVE PHASE NOISE
vs
FREQUENCY OFFSET FROM CARRIER – LVPECL

Figure 2

ADDITIVE PHASE NOISE
vs
FREQUENCY OFFSET FROM CARRIER – LVCMOS

Figure 3

jitter characteristics (continued)

AMPLITUDE PECL PEAK-TO-PEAK
vs
FREQUENCY

Mode = 1 (Divider: Y0 = 1, Y1 = 1)
Input Swing = 500 mV
Load = See Figure 11

Figure 4

AMPLITUDE CMOS PEAK-TO-PEAK
vs
FREQUENCY

Mode = 1 (divider: Y0 = 1, Y1 = 1)
Input Swing = 500 mV
Load = See Figure 10

Figure 5

supply current electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Supply current	Full load	All outputs enabled and terminated with 50 Ω to V_{DD} – 2 V on LVPECL outputs and 10 pF on LVCMOS output, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.3 V		100		mA
		No load	Outputs enabled, no output load, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.6 V			85	
I_{DDZ}	Supply current, 3-state		All outputs 3-state by control logic, f = 0 Hz, V_{DD} = 3.6 V			0.5	mA

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SUPPLY CURRENT
vs
FREQUENCY

NOTE: Input swing = 500 mV

Figure 6

Package Thermal Resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	QFN–16 package thermal resistance with thermal vias in PCB, See Note 1	4-layer JEDEC test board (JESD51–7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		40.8		°C/W

NOTE 1: It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$T_{Chassis}$ = 85°C (temperature of the chassis)

$P_{effective}$ = I_{max} x V_{max} = 85 mA x 3.6 V = 306 mW (max power consumption inside the package)

$\Delta T_{Junction}$ = θ_{JA} x $P_{effective}$ = 40.8°C/W x 306 mW = 12.48°C

$T_{Junction}$ = $\Delta T_{Junction}$ + $T_{Chassis}$ = 12.48°C + 85°C = 97.48°C (the maximum junction temperature of $T_{die-max}$ = 125°C is not violated)

TEXAS
INSTRUMENTS

CDCM1802
CLOCK BUFFER WITH PROGRAMMABLE DIVIDER,
LVPECL I/O + ADDITIONAL LVCMOS OUTPUT
SCAS759A – APRIL 2004 – JULY 2009

control input characteristics over recommended operating free-air temperature range

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{su}	Setup time, S0, S1, and EN pin before clock IN		25			ns
t_h	Hold time, S0, S1, and EN pin after clock IN		0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)			10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)			1		µs
Rpullup	Internal pullup resistor on S0, S1, and EN input		42	60	78	kΩ
$V_{IH(H)}$	Three level input high, S0, S1, and EN pin, see Note 1		$0.9 \times V_{DD}$			V
$V_{IM(M)}$	Three level input MID, S0, S1, and EN pin		$0.3 \times V_{DD}$		$0.7 \times V_{DD}$	V
$V_{IL(L)}$	Three level low, S0, S1, and EN pin				$0.1 \times V_{DD}$	V
I_{IH}	Input current, S0, S1, and EN pin	$V_I = V_{DD}$			−5	µA
I_{IL}	Input current, S0, S1, and EN pin	$V_I = GND$	38		85	µA

NOTES: 1. Leaving this pin floating automatically pulse the logic level high to V_{DD} through an internal pullup resistor of 60 kΩ.

bias voltage VBB over recommended operating free-air temperature range

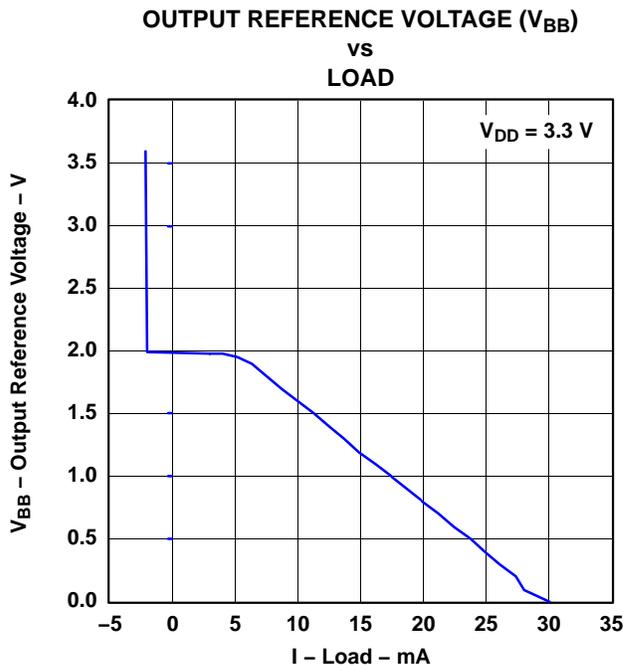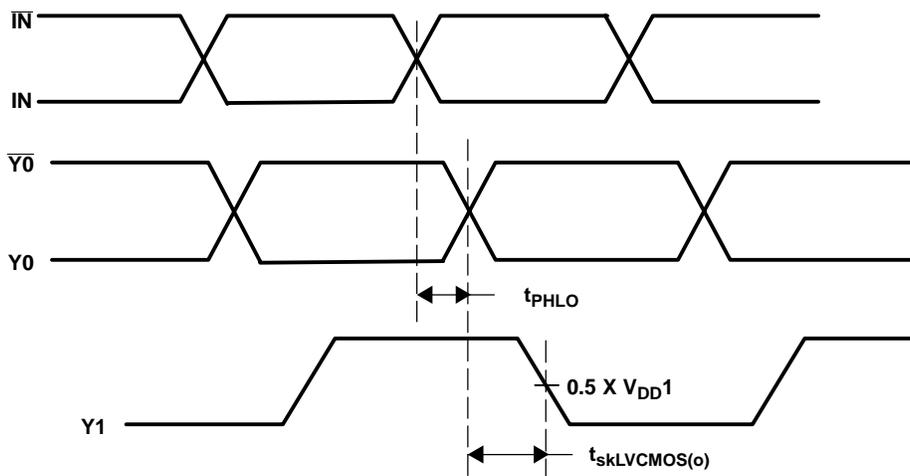|	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VBB	Output reference voltage	$V_{DD} = 3$ V – 3.6 V, $I_{BB} = -0.2$ mA	$V_{DD} - 1.4$		$V_{DD} - 1.2$	V

Figure 7

PARAMETER MEASUREMENT INFORMATION

NOTES: A. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
– The difference between the fastest and the slowest $t_{pd(LH)n}$ across multiple devices
– The difference between the fastest and the slowest $t_{pd(HL)n}$ across multiple devices

B. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL)}$) and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes Y0 to switch, $t_{sk(p)} = | t_{pd(HL)} - t_{pd(LH)} |$. Pulse skew is sometimes referred to as *pulse width distortion* or *duty cycle skew.*

Figure 8. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$
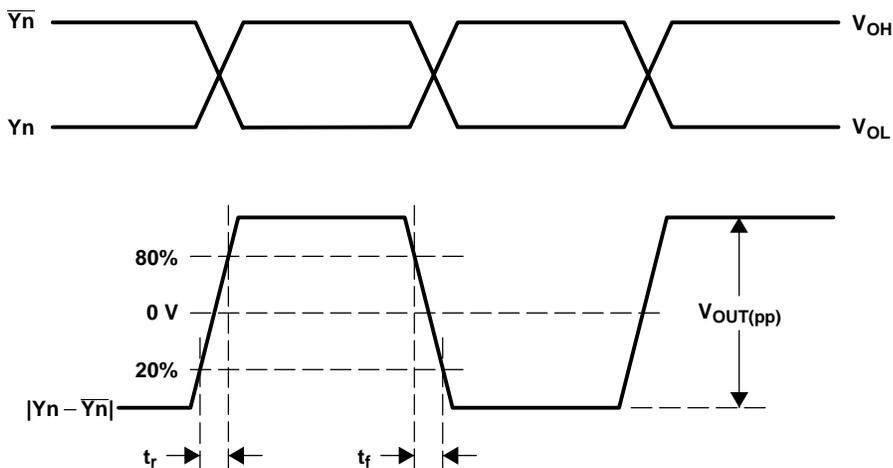
Figure 9. LVPECL Differential Output Voltage and Rise/Fall Time
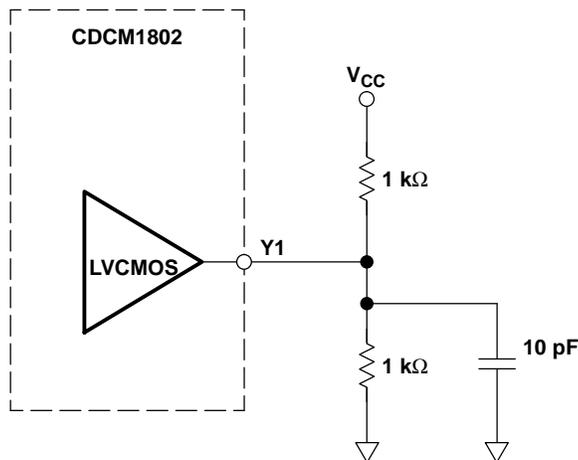
PARAMETER MEASUREMENT INFORMATION

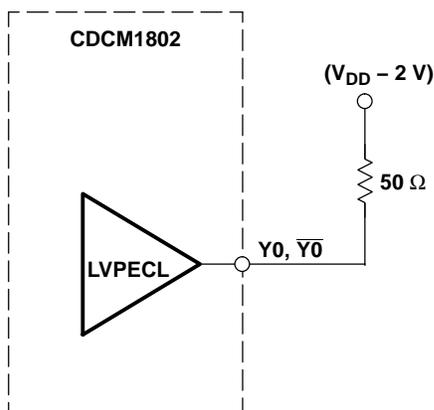**Figure 10. LVCMOS Output Loading During Device Test**

Figure 11. LVPECL Output Loading During Device Test

PCB design for thermal functionality

It is recommended to take special care of the PCB design for good thermal flow from the QFN–16 pin package to the PCB. The current consumption of the CDCM1802 is fixed. JEDEC JESD51–7 specifies thermal conductivity for standard PCB boards.

Modeling the CDCM1802 with a 4–layer JEDEC board (including four thermal vias) results into 37.5°C max temperature with a θ_{JA} of 40.84°C for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications.

PARAMETER MEASUREMENT INFORMATION

**Package Thermal Pad
(Underside)**

**Thermal Via
Dia 0.020 In.**

**Top Side
Island**

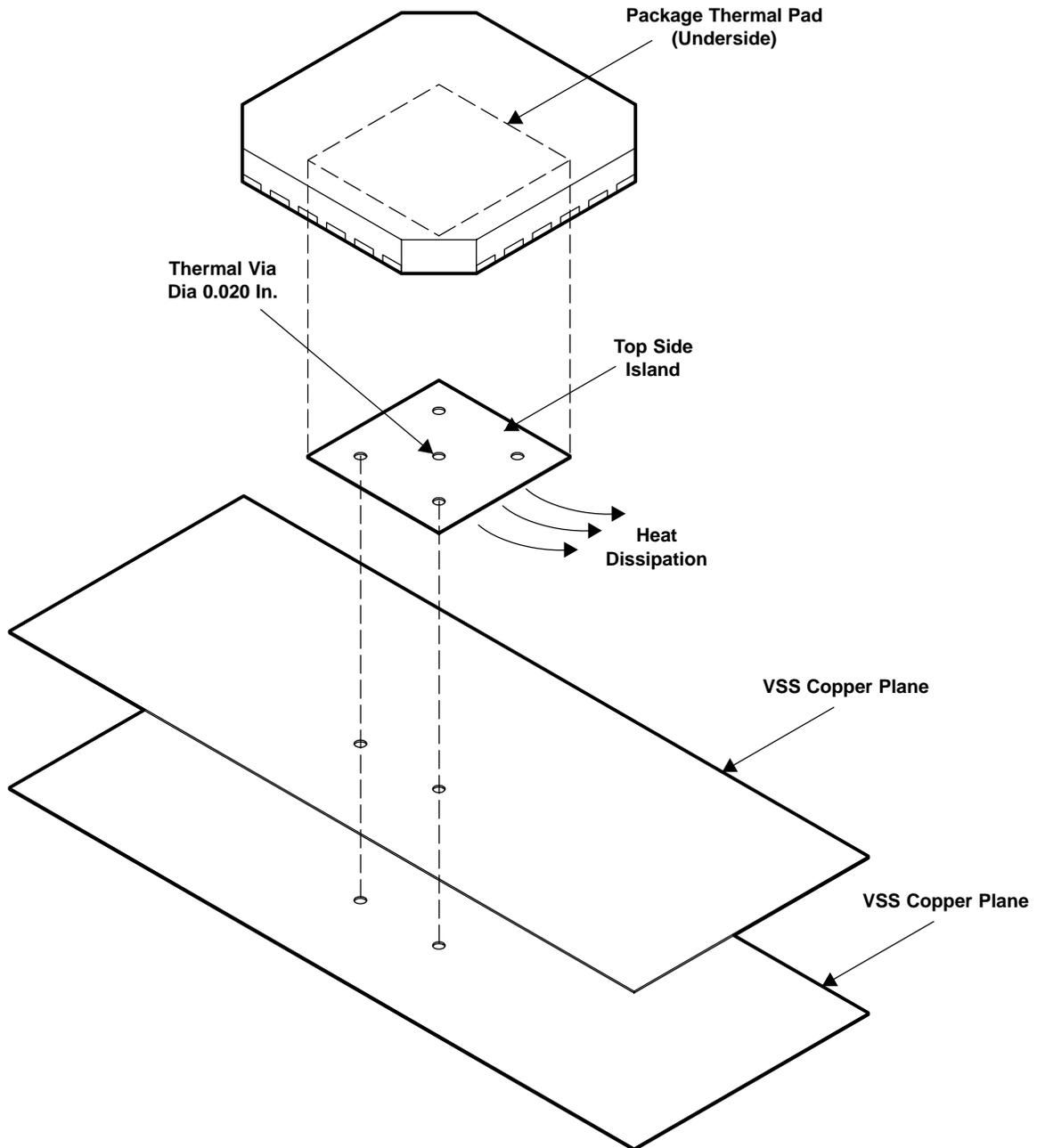**Heat
Dissipation**

VSS Copper Plane

VSS Copper Plane

Figure 12. Recommended Thermal Via Placement

See the SCBA017 and the SLUA271 application notes for further package related information.

APPLICATION INFORMATION

LVPECL receiver input termination

The input of the CDCM1802 has high impedance and comes with a very large common mode voltage range. For optimized noise performance it is recommended to properly terminate the PCB trace (transmission line).

Additional termination techniques can be found in the following application notes: SCAA062 and SCAA059.

http://focus.ti.com/docs/apps/catalog/resources/appnoteabstract.jhtml?abstractName=scaa062

http://focus.ti.com/docs/apps/catalog/resources/appnoteabstract.jhtml?abstractName=scaa059
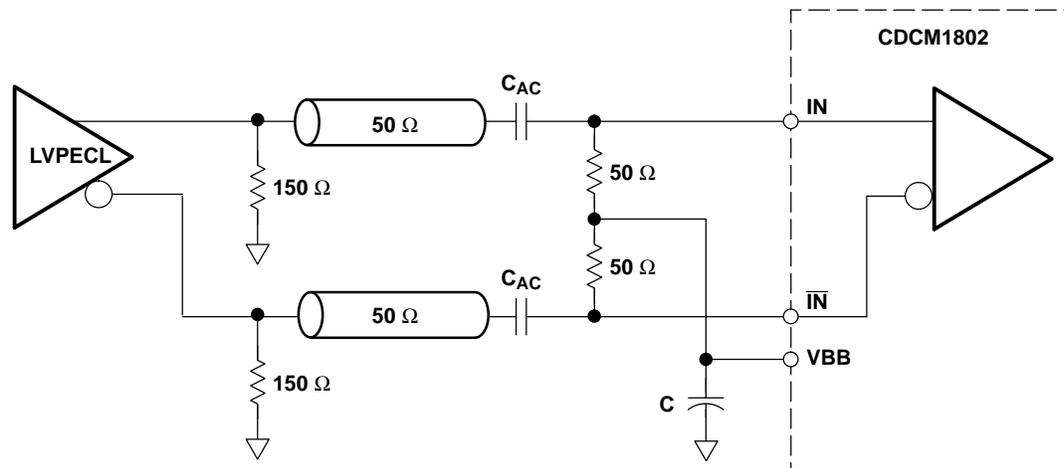

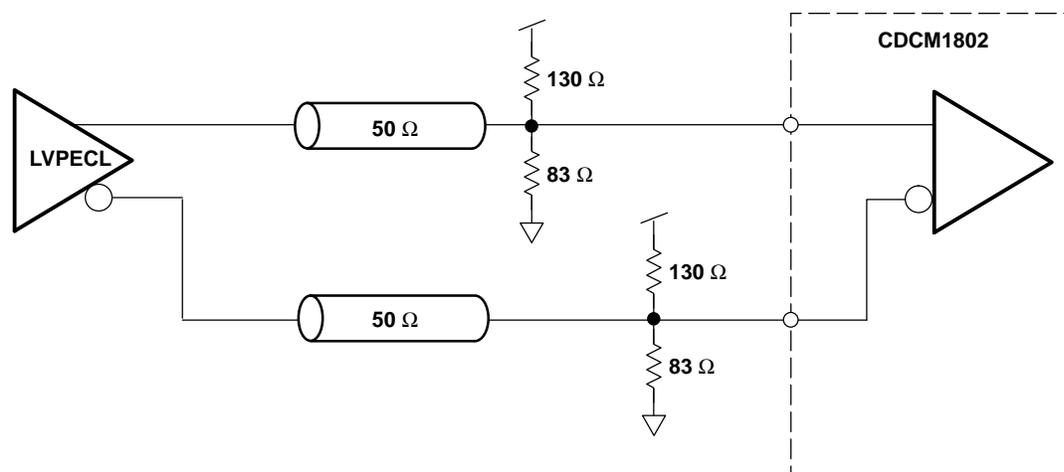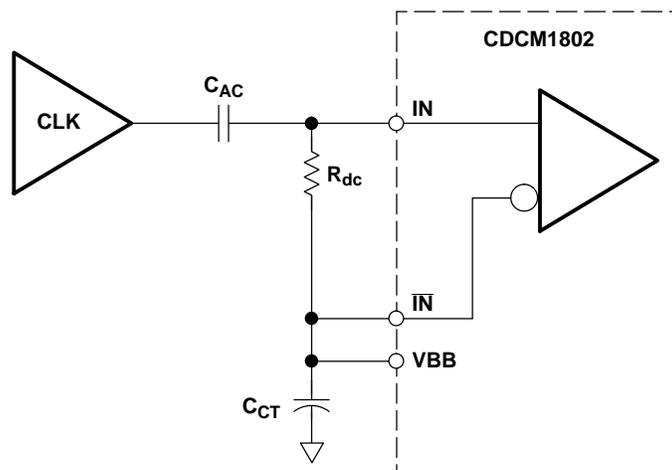**Figure 13. Recommended AC-Coupling LVPECL Receiver Input Termination**

Figure 14. Recommended DC-Coupling LVPECL Receiver Input Termination

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

NOTE: C_{AC} – AC-coupling capacitor (e.g., 10 nF)
C_{CT} – Capacitor keeps voltage at $\overline{IN}$ constant (e.g., 10 nF)
R_{dc} – Load and correct duty cycle (e.g., 50 Ω)
V_{BB} – Bias voltage output

Figure 15. Typical Application Setting for Single-Ended Input Signals Driving the CDCM1802

device behavior during RESET and control pin switching

output behavior when enabling the device (EN = 0 $\Rightarrow$ 1)

In disable mode (EN = 0), all output drivers are switched in high-Z mode. The bandgap, current references, the amplifier, and the S0 and S1 control inputs are also switched off. In the same mode, all flip-flops will be reset. The typical current consumption is likely below 500 μA (to be measured).

When the device will be enabled again it takes maximal 1 μs for the settling of the reference voltage and currents. During this time the output Y0 and $\overline{Y0}$ drive a high signal. Y1 is unknown (could be high or low). After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device look like those shown in Figure 16. The inverting input and output signal is not included. The Y:/1 waveform is the undivided output driver state.

APPLICATION INFORMATION
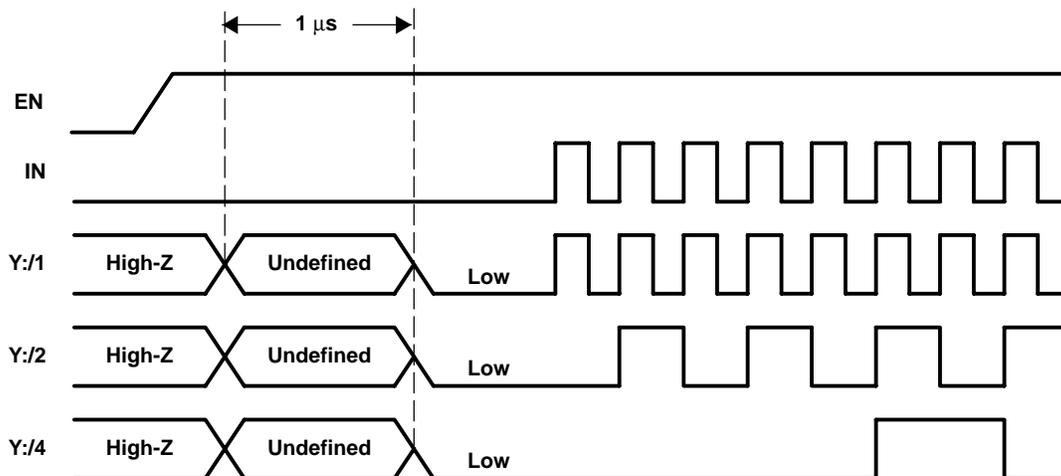
Signal State After the Device is Enabled (IN = Low)
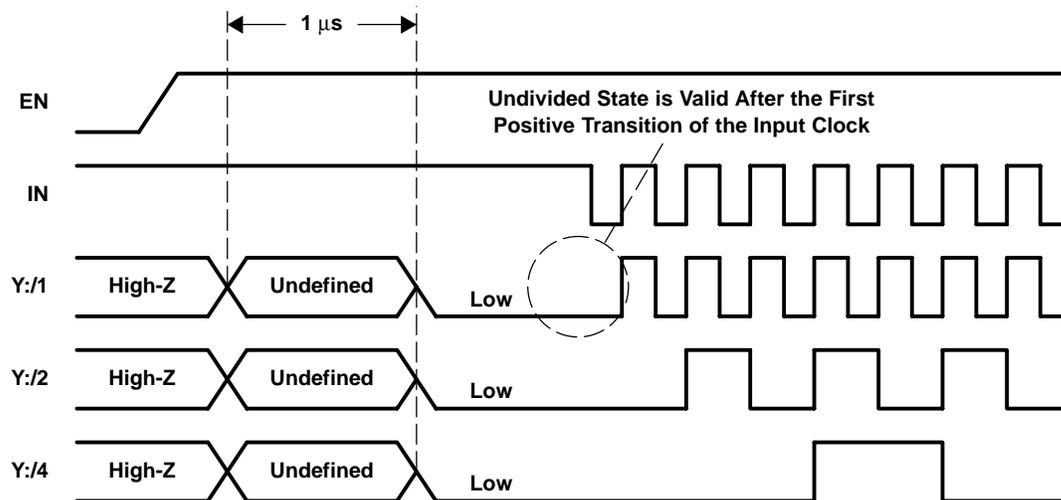
Signal State After the Device is Enabled (IN = High)

Figure 16. Waveforms

APPLICATION INFORMATION

enabling a single output stage

If a single output stage becomes enabled:

1. Y0 will either be low or high (undefined).

2. $\overline{Y0}$ will be the inverted signal of Y0.

With the first positive clock transition, the undivided output becomes the input clock state. If a divide mode is used, the divided output states are equal to the actual internal divider. The internal divider does not get a reset while enabling single output drivers.
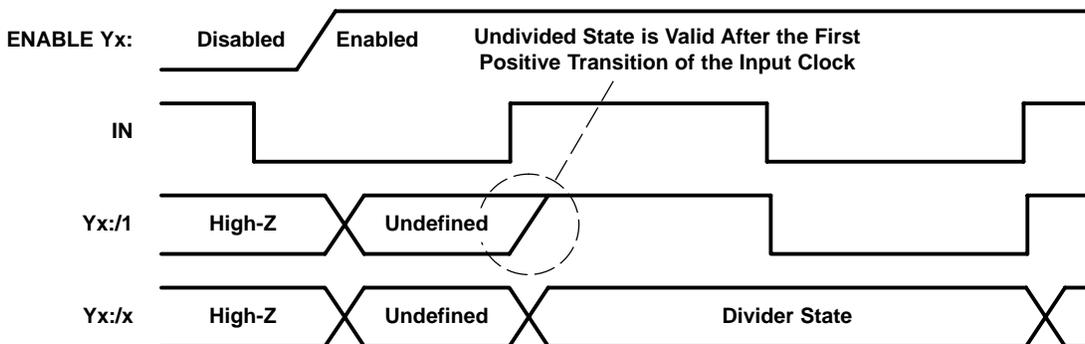
Figure 17. Signal State After an Output Driver Becomes Enabled While IN = 0
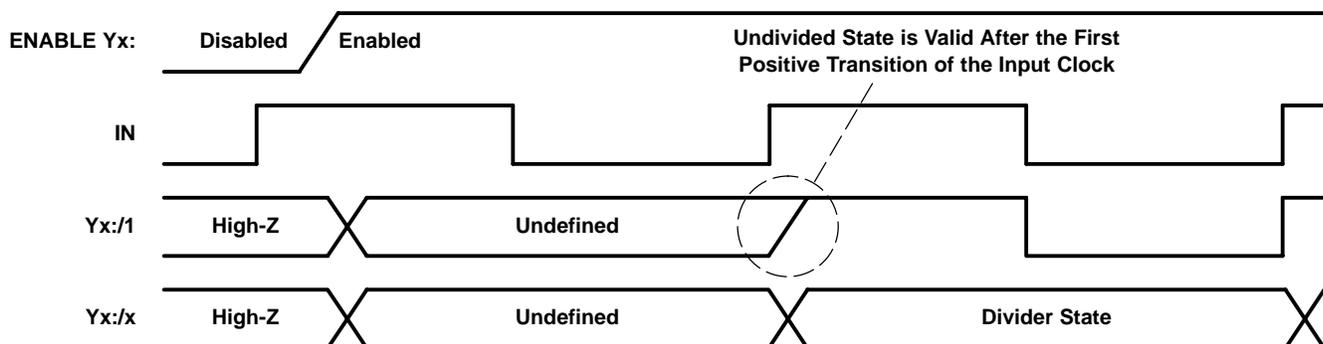
Figure 18. Signal State After an Output Driver Becomes Enabled While IN = 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCM1802RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples
CDCM1802RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples
CDCM1802RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples
CDCM1802RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AJW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
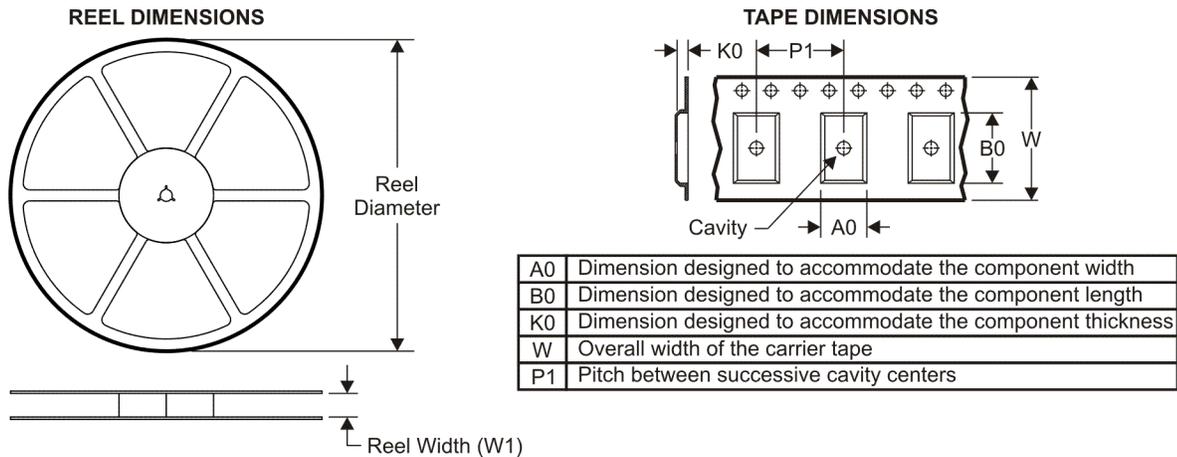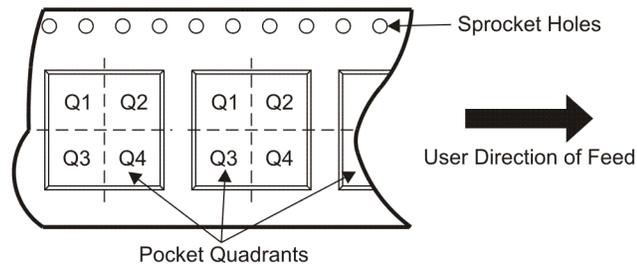
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM1802RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q2
CDCM1802RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q2

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION
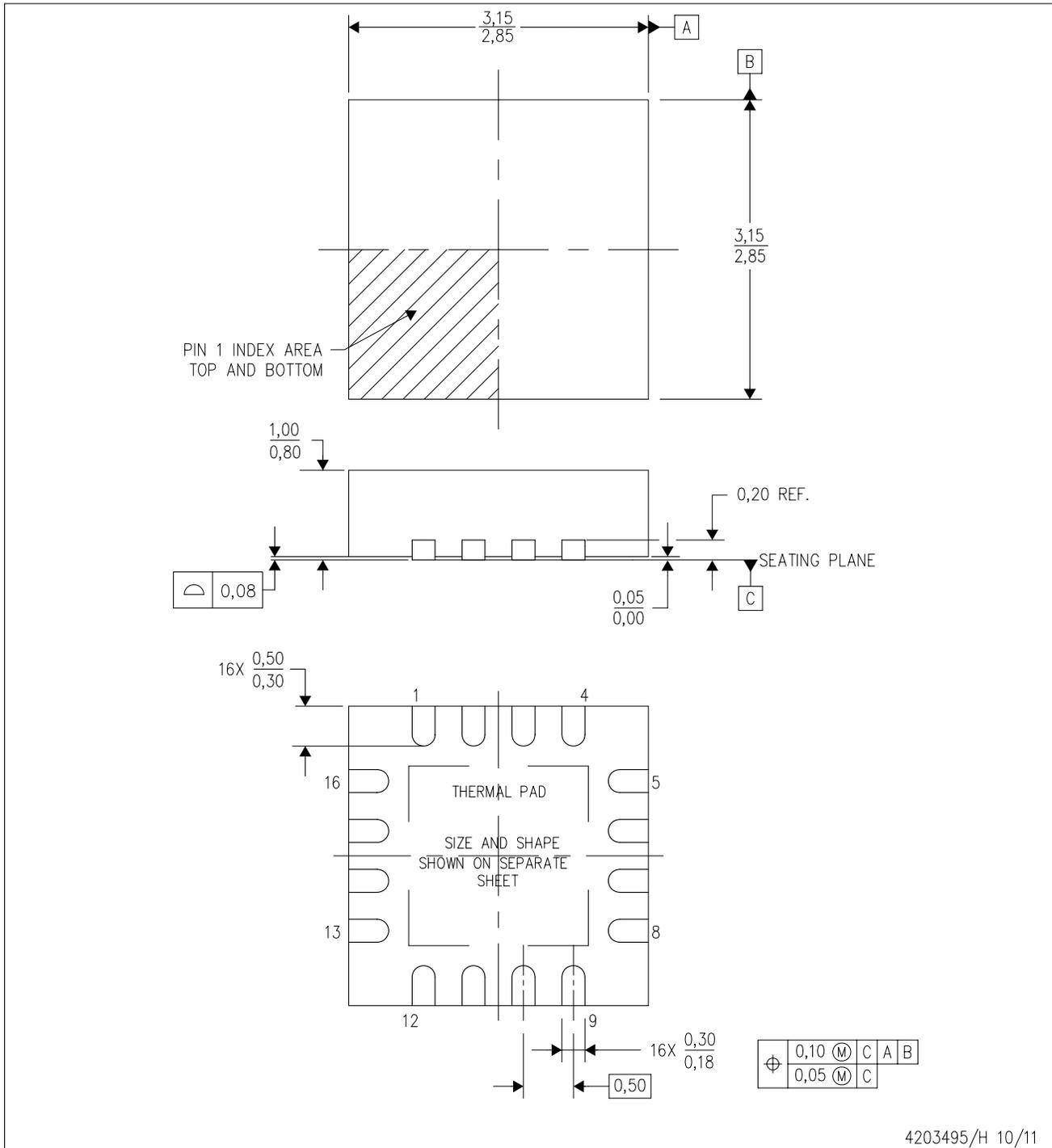
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM1802RGTR	QFN	RGT	16	3000	340.5	338.1	20.6
CDCM1802RGTT	QFN	RGT	16	250	340.5	338.1	20.6

RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{3,15}{2,85}$ A

B

$\frac{3,15}{2,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

⌓ 0,08

$\frac{0,05}{0,00}$ C

16X $\frac{0,50}{0,30}$

1   4

16   5

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE
SHEET

13   8

12   9

16X $\frac{0,30}{0,18}$

0,50

⊕ | 0,10 Ⓜ | C | A | B
0,05 Ⓜ | C

4203495/H 10/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Falls within JEDEC MO−220.

TEXAS INSTRUMENTS
www.ti.com

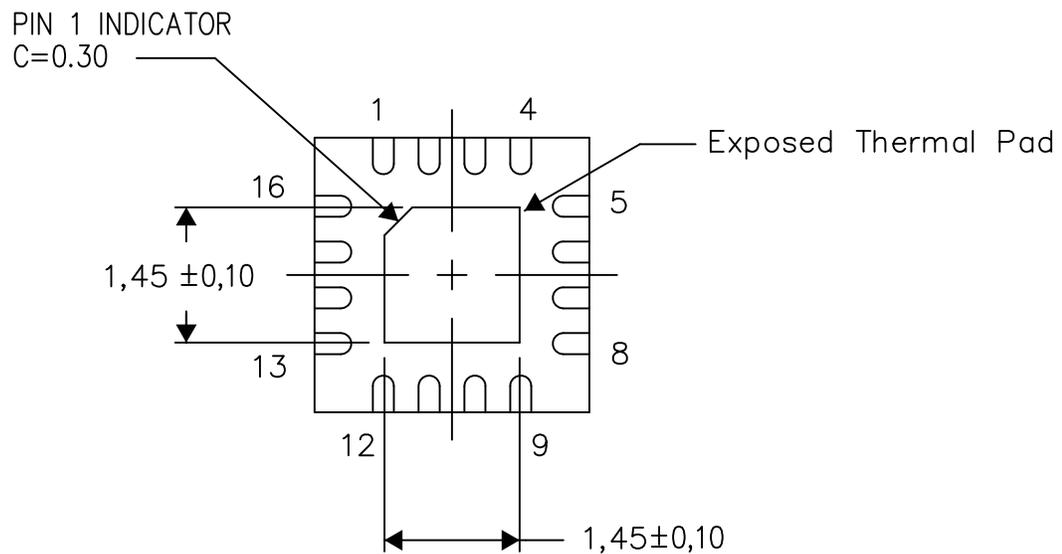RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C=0.30

Exposed Thermal Pad

1,45 ±0,10

1,45±0,10

Bottom View
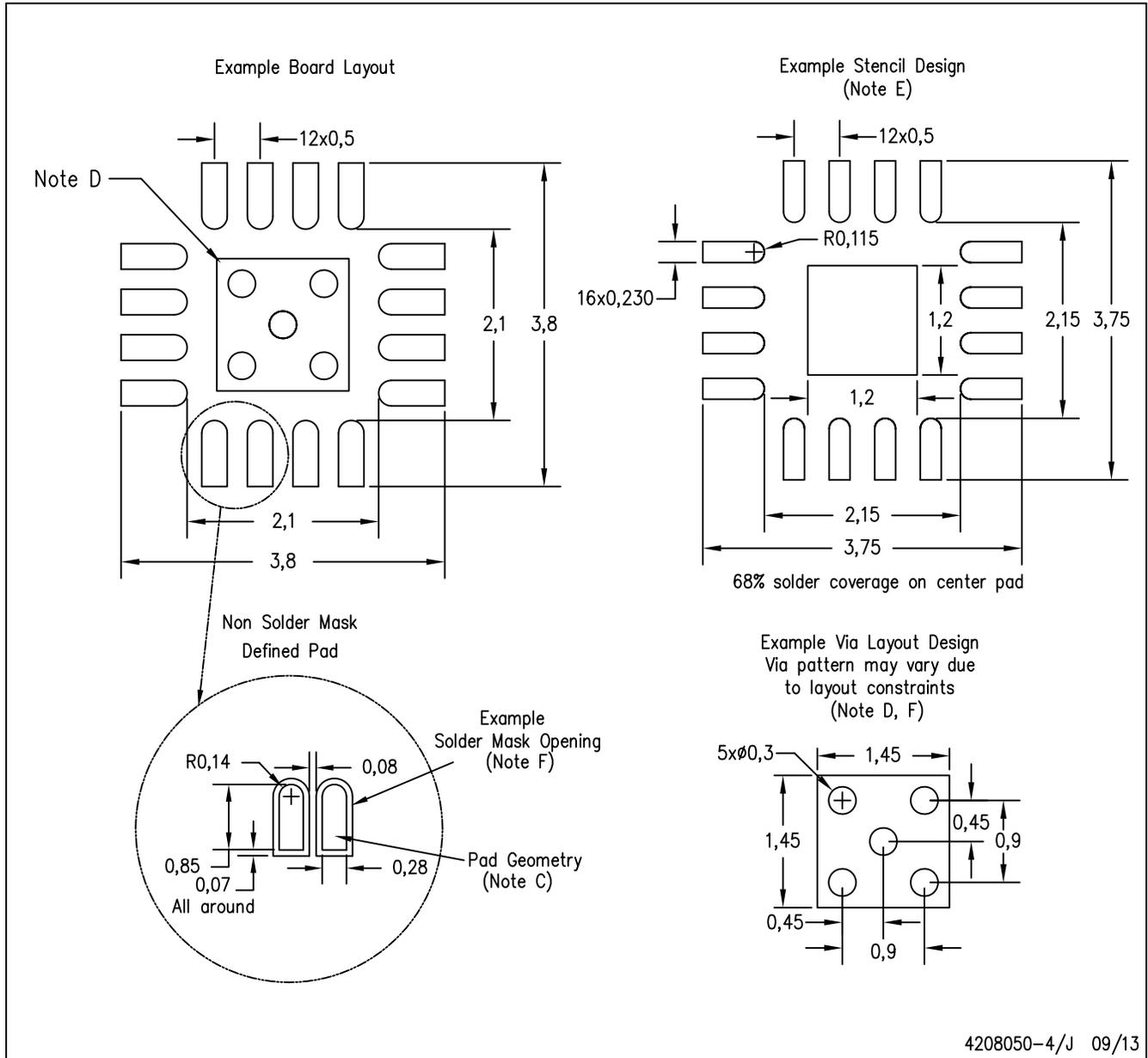
Exposed Thermal Pad Dimensions

4206349−2/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note D

12x0,5

2,1 3,8

2,1

3,8

Non Solder Mask
Defined Pad

R0,14   0,08

0,85
0,07
All around

0,28

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

Example Stencil Design
(Note E)

12x0,5

R0,115

16x0,230

1,2

1,2

2,15 3,75

2,15

3,75

68% solder coverage on center pad

Example Via Layout Design
Via pattern may vary due
to layout constraints
(Note D, F)

5xØ0,3   1,45

1,45

0,45

0,45   0,9

0,9

0,45

4208050−4/J   09/13

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

**TEXAS
INSTRUMENTS**
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated