

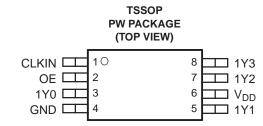
200-MHz GENERAL-PURPOSE CLOCK BUFFER, PCI-X COMPLIANT

Check for Samples: CDCV304

FEATURES

- General-Purpose and PCI-X 1:4 Clock Buffer
- Operating Frequency
 - 0 MHz to 200 MHz General-Purpose
- Low Output Skew: <100 ps
- Distributes One Clock Input to One Bank of Four Outputs
- Output Enable Control that Drives Outputs Low when OE is Low
- Operates from Single 3.3-V Supply or 2.5-V Supply

- PCI-X Compliant
- 8-Pin TSSOP Package



DESCRIPTION

The CDCV304 is a high-performance, low-skew, general-purpose PCI-X compliant clock buffer. It distributes one input clock signal (CLKIN) to the output clocks (1Y[0:3]). It is specifically designed for use with PCI-X applications. The CDCV304 operates at 3.3 V and 2.5 V and is therefore compliant to the 3.3-V PCI-X specifications.

The CDCV304 is characterized for operation from -40°C to 85°C for automotive and industrial applications.

FUNCTIONAL BLOCK DIAGRAM

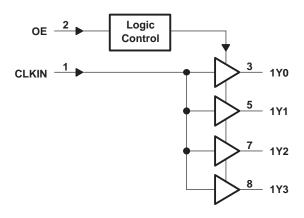


Table 1. FUNCTION TABLE

INP	OUTPUTS	
CLKIN	1Y[0:3]	
L	L	L
Н	L	L
L	Н	L
Н	Н	Н



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION			
NAME	NO.	1/0	DESCRIPTION			
1Y[0:3]	3, 5, 7, 8	0	Buffered output clocks			
CLKIN	1	I	Input reference frequency			
GND	4	Power	Ground			
OE	2	I	Output enable control			
V_{DD}	6	Power	Supply			

THERMAL INFORMATION(1)

	CDCV204DW 9 DIN TCCOD		THI	ERMAL AIF	UNIT		
	CDCV304PW 8-PIN TSSOP				250	500	UNII
$R_{\theta JA}$	High K		149	142	138	132	
$R_{\theta JA}$	Low K		230	185	170	150	
$R_{\theta JB}$	High K	102.0					°C 111
R_{\thetaJC}	High K	43.7					°C/W
ΨJT	High K	1.8					
Ψ ЈВ	High K	100.2					

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	UNIT
Supply voltage range, V _{DD}	–0.5 V to 4.3 V
Input voltage range, V _I (2) (3)	$-0.5 \text{ V to V}_{DD} + 0.5 \text{ V}$
Output voltage range, V _O ^{(2) (3)}	–0.5 V to V _{DD} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±50 mA
Continuous total output current, I _O (V _O = 0 to V _{DD})	±50 mA
Package thermal impedance, θ _{JA} : PW package	230.5°C/W
Storage temperature range T _{stg}	−65°C to 150°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This value is limited to 4.6 V maximum.



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM MAX	UNIT
Supply voltage, V _{DD}		2.3	3.6	V
Low-level input voltage, V _{IL}			0.3 x V _{DD}	V
High-level input voltage, V _{IH}		0.7 x V _{DD}		V
Input voltage, V _I		0	V_{DD}	V
High level evitant evinent I	V _{DD} = 2.5 V		-12	
nigh-level output current, I _{OH}	V _{DD} = 3.3 V		-24	mA
Lavidaval autout aumant 1	V _{DD} = 2.5 V		12	
cow-level input voltage, V_{IL} 0.3 x V_{DD} digh-level input voltage, V_{IH} 0.7 x V_{DD} 10 V_{DD} 11 V_{DD} 12 V_{DD} 13 V_{DD} 15 V_{DD} 16 V_{DD} 17 V_{DD} 17 V_{DD} 18 V_{DD} 19	mA			
Operating free-air temperature, T				°C

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{clk}	Clock frequency		0		200	MHz

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	ONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IK}	Input voltage	$V_{DD} = 3 V$,	$I_1 = -18 \text{ mA}$			-1.2	V	
		V _{DD} = 2.3 V,	$I_{OH} = -8 \text{ mA}$	1.8				
		$V_{DD} = 2.3 V,$	I _{OH} = -16 mA	1.5				
V_{OH}	High-level output voltage	$V_{DD} = min to max,$	$I_{OH} = -1 \text{ mA}$	V _{DD} – 0.2			V	
		$V_{DD} = 3 V$,	$I_{OH} = -24 \text{ mA}$	2				
		$V_{DD} = 3 V$,	$I_{OH} = -12 \text{ mA}$	2.4				
		V _{DD} = 2.3 V,	I _{OL} = 8 mA			0.5		
		$V_{DD} = 2.3 \text{ V}, \qquad I_{OL} = 16 \text{ mA}$		0.7				
V_{OL}	Low-level output voltage	$V_{DD} = min to max,$	$I_{OL} = 1 \text{ mA}$			0.2	V	
		$V_{DD} = 3 \text{ V}, \qquad \qquad I_{OL} = 24 \text{ mA}$			8.0			
		$V_{DD} = 3 V$,	I_{OL} = 12 mA			0.55		
	High level output ourrent	$V_{DD} = 3 V$,	V _O = 1 V	-50				
I _{OH}	High-level output current	$V_{DD} = 3.3 V,$	V _O = 1.65 V		– 55		mA	
	I am laval antonit annout	V _{DD} = 3 V,	V _O = 2 V	60			A	
l _{OL}	Low-level output current	$V_{DD} = 3.3 \text{ V},$	V _O = 1.65 V	70			mA	
I _I	Input current	$V_I = V_O \text{ or } V_{DD}$				±5	μΑ	
	Dunamia aumant and Figure 5	f = 67 MHz,	V _{DD} = 2.7 V			28	A	
I _{DD}	Dynamic current, see Figure 5	f = 67 MHz,	V _{DD} = 3.6 V			37	mA	
Cı	Input capacitance	$V_{DD} = 3.3 \text{ V},$	$V_I = 0 \text{ V or } V_{DD}$		3		pF	
Co	Output capacitance	$V_{DD} = 3.3 \text{ V},$	$V_I = 0 \text{ V or } V_{DD}$		3.2		pF	

⁽¹⁾ All typical values are with respect to nominal V_{DD} and T_A = 25°C.

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SWITCHING CHARACTERISTICS

 V_{DD} = 2.5 V ± 10%, C_L = 10 pF (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Low-to-high propagation delay	See Figure 4 and Figure 2	2	2.9	4.5	20
t _{PHL}	High-to-low propagation delay	See Figure 1 and Figure 2	2	3	4.5	ns
t _{sk(o)}	Output skew ⁽²⁾	See Figure 3		50	150	ps
t _r	Output rise slew rate		1.5	2.2	4	V/ns
t _f	Output fall slew rate		1.5	2.2	4	V/ns

SWITCHING CHARACTERISTICS

 V_{DD} = 3.3 V ± 10%, C_L = 10 pF (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
t _{PLH}	Low-to-high propagation delay	See Figure 4 and Figure 2	1.8	2.4	3		
t _{PHL}	High-to-low propagation delay	See Figure 1 and Figure 2	1.8	2.5	3	ns	
t _{sk(o)}	Output skew ⁽²⁾			50	100	ps	
	Additional base little frame input to autout 400	12 kHz to 5 MHz, f _{out} = 30.72 MHz		63		f	
t _{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 20 MHz, f _{out} = 125 MHz		56		fs rms	
t _{sk(p)}	Pulse skew	$V_{IH} = V_{DD}, V_{IL} = 0 V$			150	ps	
t _{sk(pr)}	Process skew			0.2	0.3	ns	
t _{sk(pp)}	Part-to-part skew			0.25	0.4	ns	
	Clash kink time and Figure 4	66 MHz	6				
t _{high}	Clock high time, see Figure 4	140 MHz	3			ns	
	Clash law times and Figure 4	66 MHz	6				
t _{low}	Clock low time, see Figure 4	140 MHz	3			ns	
t _r	Output rise slew rate ⁽³⁾	V _O = 0.4 V to 2 V	1.5	2.7	4	V/ns	
t _f	Output fall slew rate ⁽³⁾	V _O = 2 V to 0.4 V	1.5	2.7	4	V/ns	

All typical values are with respect to nominal V_{DD} . The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

 $[\]begin{array}{ll} \text{(1)} & \text{All typical values are with respect to nominal V_{DD}.} \\ \text{(2)} & \text{The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.} \\ \text{(3)} & \text{This symbol is according to PCI-X terminology.} \end{array}$



PARAMETER MEASUREMENT INFORMATION

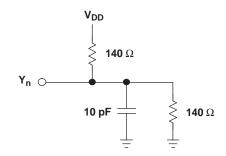


Figure 1. Test Load Circuit

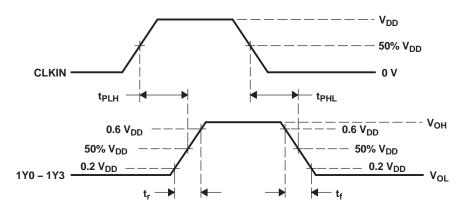


Figure 2. Voltage Waveforms Propagation Delay (tpd) Measurements

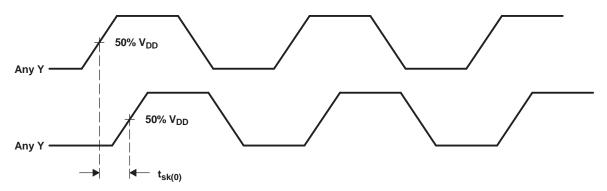
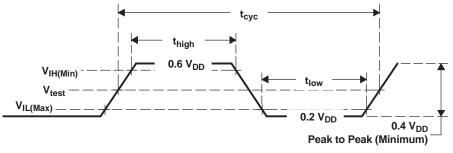


Figure 3. Output Skew

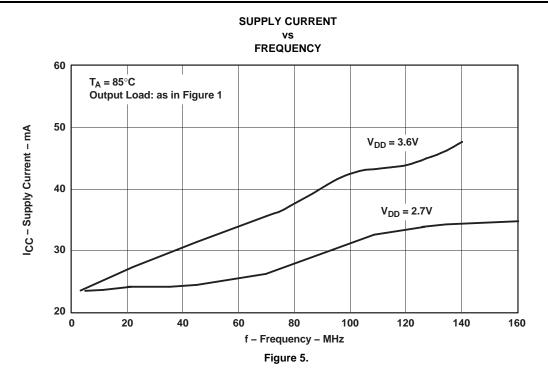
PARAMETER	VALUE	UNIT
$V_{IH(Min)}$	$0.5~V_{DD}$	V
V _{IL(Max)}	$0.35~\mathrm{V_{DD}}$	V
V _{test}	0.4 V _{DD}	V



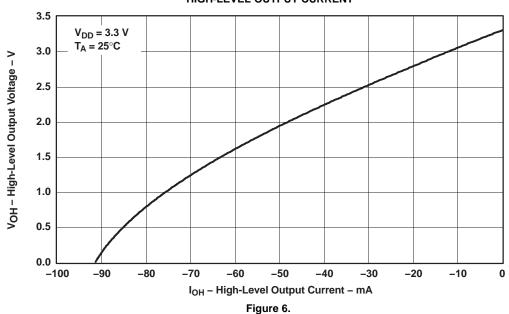
A. All parameters in Figure 4 are according to PCI-X 1.0 specifications.

Figure 4. Clock Waveform





HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT





LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

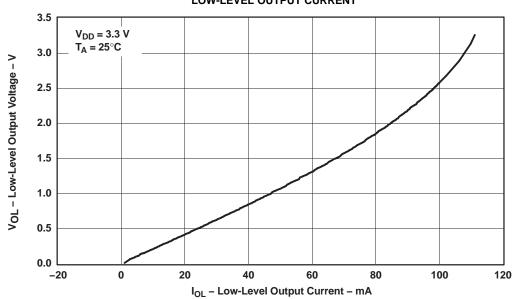


Figure 7.



REVISION HISTORY

C	hanges from Revision F (April 2009) to Revision G	Page
•	Added ψ _{JT} and ψ _{JB} specs to the Thermal Information Table and changed R _{θJB} and R _{θJC} specs from 65 and 69 °C/W respectively.	2
C	hanges from Revision G (January 2011) to Revision H	Page
	Added missing characteristics graphs.	6





14-Jan-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CDCV304PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	Level-1-260C-UNLIM	-40 to 85	CKV304	Samples
CDCV304PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV304	Samples
CDCV304PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	Level-1-260C-UNLIM	-40 to 85	CKV304	Samples
CDCV304PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV304	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

14-Jan-2016

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OTHER QUALIFIED VERSIONS OF CDCV304:

■ Enhanced Product: CDCV304-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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